Evaluating Cache Power Dissipation using CACTI 5.3 simulator

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Outline

- Introduction .
- Cacti 5.3 Simulator.
- Simulation results.
- Conclusions.
- Future works.

Introduction

- Power dissipation has become a major concern to those designers for high performance microprocessors.
- Power dissipation Types:
  1. Dynamic power
  2. Static Power (leakage).

Where

$$Total\ Power = Dynamic\ Power + Leakage\ Power$$

CACTI 5.3 SIMULATOR

- CACTI 5.3 is the latest version of CACTI
- CACTI is an integrated cache access time, cycle time, area, leakage, and dynamic power model

Technology Modeling

- CACTI 5.3 makes use of technology projections from the ITRS.

- Four ITRS technology nodes
  - 90 nm
  - 65 nm
  - 45 nm
  - and 32 nm

  which cover years 2004 to 2013 in the ITRS.

Results

- 32kB 2-way set-associative caches with 32-byte cache lines

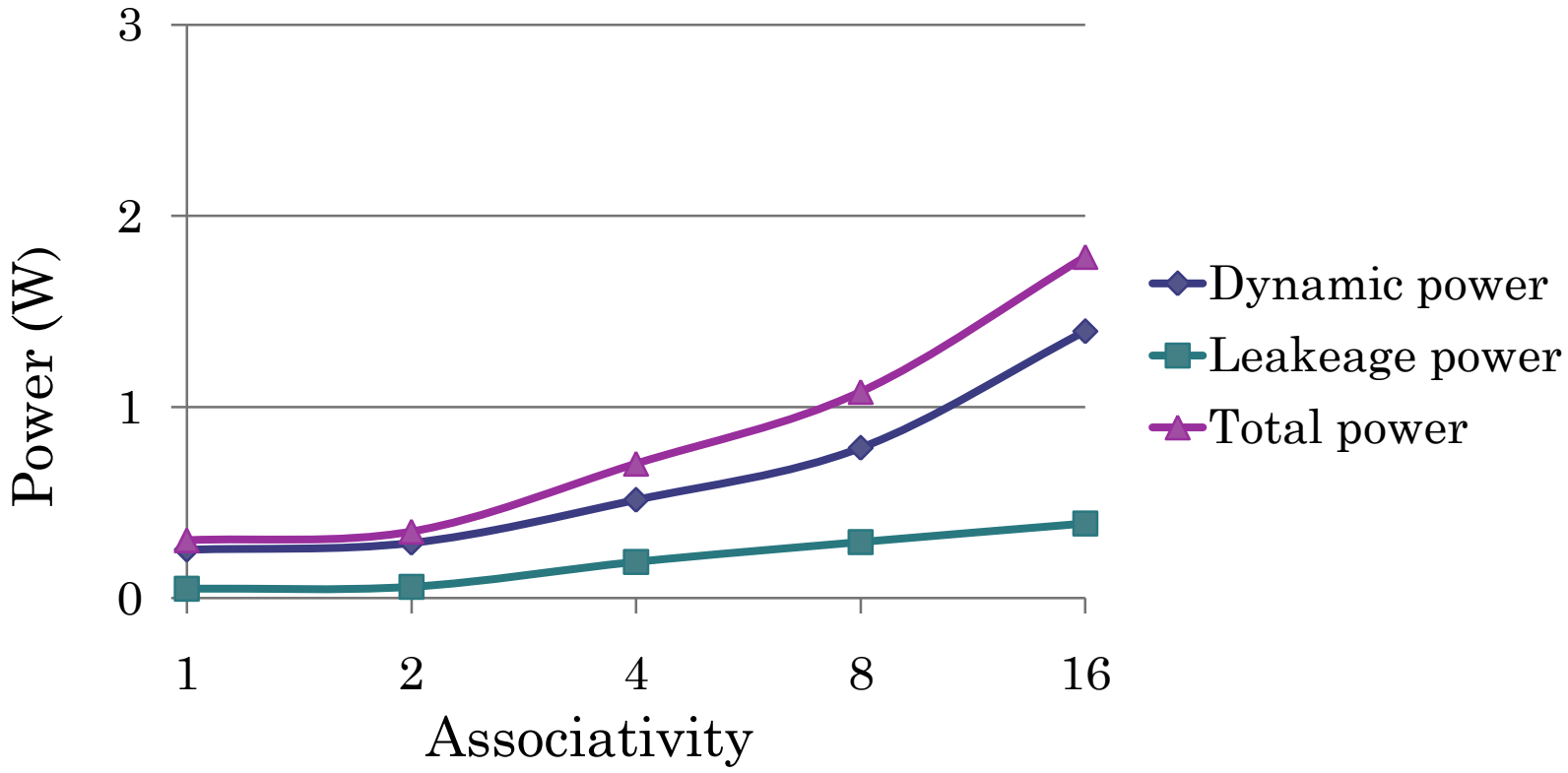
Technology [nm]	32	45	65	90
Access time [nsec]	0.64	0.828	1.392	1.84
Dynamic energy [nJ]	.041	0.071	0.107	.16

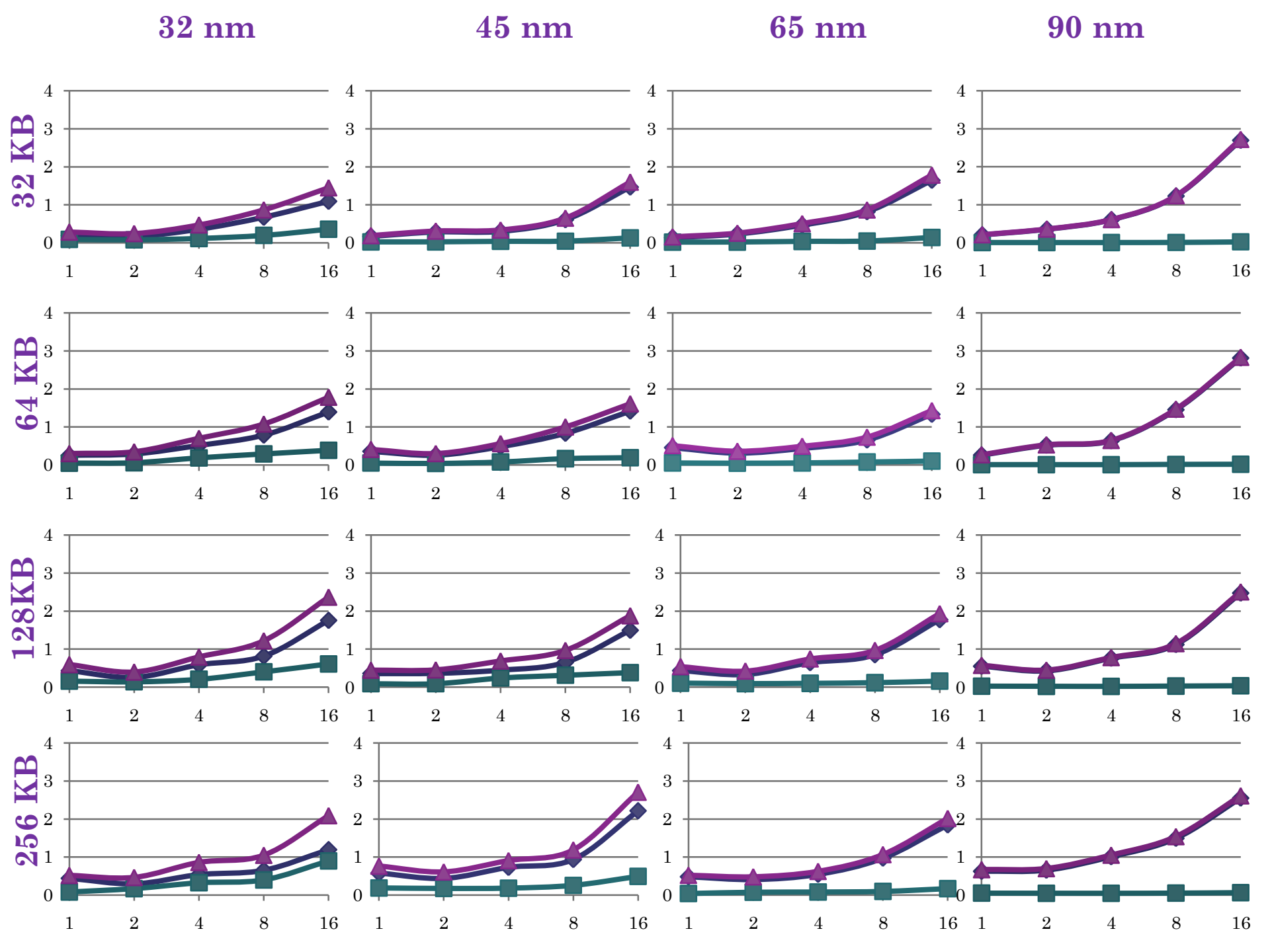
- Where

  Dynamic Power = Dynamic energy(nJ)/ Cycle Time(ns)

Results

- 64KB caches with
  - 64-byte cache lines.
  - 32 nm node technology.




32 nm
45 nm
65 nm
90 nm
32 KB
64 KB
128KB
256 KB
0
1
2
3
4
1
2
4
8
16

Conclusions

- Total power is dominated by dynamic power in highly associative larger nanometer technologies
- As transistors become smaller with improving fabrication process technologies, device leakage power dissipation become a major concern in new cache designs

Future works

- Techniques to limit power consumption:

- Turn off cache lines that are not used for long time
- Use low power supply voltages

Thank You