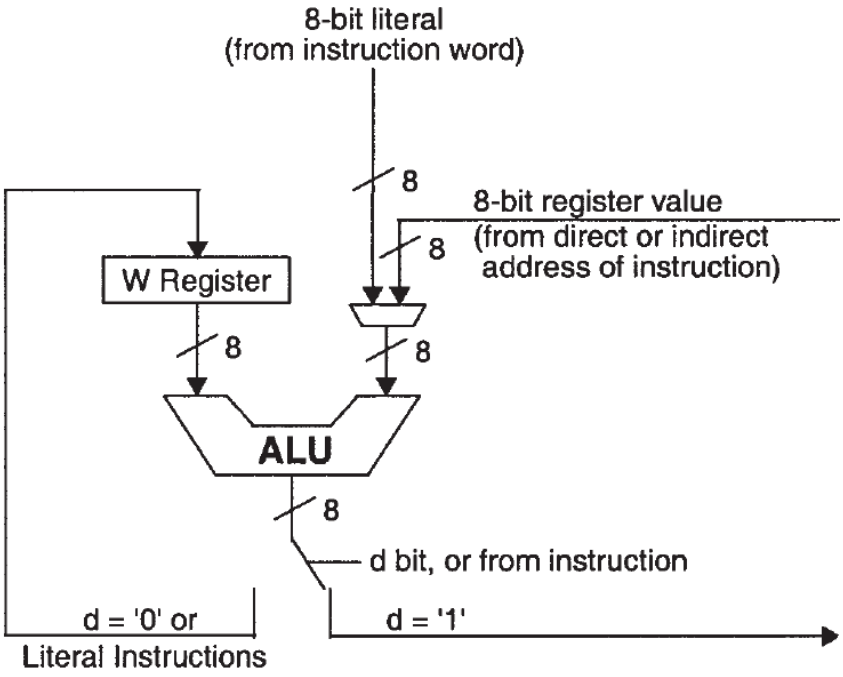
University of Jordan
Computer Engineering Department
CPE439: Computer Design Lab

Experiment 4: Datapath

It is required to construct and test a Verilog module for a datapath suitable for incorporation in your PIC16F84A design. This datapath should use the ALU you have built in Experiment 3. You should use modular design where you start by building and testing low-level modules using the library modules defined in **Lib439.v**, then use the low-level modules in larger modules. The following figure shows the design of this datapath.



8-bit Register

The W register should be built using eight **DFF** modules defined in the library **Lib439.v**. You need a way to implement an active-high `enable` input for this register. The 8-bit register implementation should be similar to the following code:

```
module Register_8b (Q, D, clk, reset, enable);
  output [7,0] Q;
  input [7,0] D;
  input clk, reset, enable;
  // implementation details are left to the student
  …
endmodule
```

Datapath Module

The datapath module should have Verilog code similar to the following code:

```
module Datapath(Result, C, DC, Z, L, F, m, b, Cin, x, L_or_F, d, clk, reset);
  output [7:0] Result;
  output C, DC, Z;
  input [7:0] L, F;
  input [3:0] m;
  input [2:0] b;
  input Cin, x;
  input L_or_F;        //0 input from instruction, 1 input from register
  input d;             //0 result to W, 1 result to register
  input clk, reset;
  // implementation details are left to the student
  …
endmodule
```

Report

Your report should include detailed design, Verilog code for all modules including your test modules, and timing diagram that demonstrates the correct operation of your design given the input shown in the following table. Also estimate the maximum delay expected for you design.

L	F	m	b	Cin	x	L_or_F	d	clk	reset
0101 1001	0011 1001	0000	000	0	0	0	0	0 to 1 to 0	1
0101 1001	0111 1111	0000	000	0	0	1	0	0 to 1 to 0	0
0101 1001	0011 1001	0001	000	0	0	1	1	0 to 1 to 0	0
0101 1001	1000 0000	1101	000	0	0	0	0	0 to 1 to 0	0
0101 1001	0111 1111	1010	000	1	0	1	0	0 to 1 to 0	0
0101 1001	0111 1111	1110	010	0	1	0	0	0 to 1 to 0	0