University of Jordan
Computer Engineering Department
CPE439: Computer Design Lab

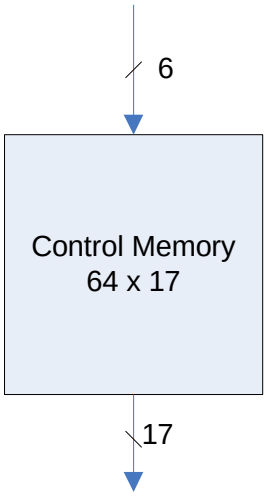
Experiment 9: The Control Module

It is required to construct a Verilog module for a control unit suitable for incorporation in your PIC16F84A design. This unit should provide the control signals needed to implement the instructions summarized in Table 1. This table specifies, for every instruction, its description, execution time in cycles, instruction format, and the affected status flags.

Table 1: PIC16F84A Instruction Set (modified)

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected
BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff	
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff	
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z
MOVWF	f	Move W to f	1	00	0000	lfff	ffff	
NOP	-	No Operation	1	00	0000	0xxx	xxxx	
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff	
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff	
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff	
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff	
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff	
LITERAL AND CONTROL OPERATIONS								
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk	
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk	
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk	
RETURN	-	Return from Subroutine	2	11	1011	xxxx	xxxx	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z

This control unit can simply be implemented using a ROM. As shown in the figure below, the size of this control memory is sixty four 17-bit locations. The input to this memory consists of the six most significant bits of the fetched instructions IR_Data[13:8]. These six bits are used as an address to access one 17-bit location that contains the control signals of the fetched instruction. This memory should be implemented inside the control module using behavioral modeling similar to the module used to implement the flash program memory in Experiment 5.



The control module should have Verilog code similar to the following code:

```
module Conrol(Instr, W_write, Write_en, m, L_or_F,
              F_write, C_en, DC_en, Z_en,
              IR_clear, IR_clear_cond, PC_Sel, Push, Pop);
  input [5:0] Instr;
  output W_write;       //active for instructions that write into W
  output Write_en;      //active for instructions that write into W or F
  output [3:0] m;
  output L_or_F;
  output F_write;       //active for instructions that write into F
  output C_en, DC_en, Z_en;
  output IR_clear;      //active for jump instructions
  output IR_clear_cond; //active for conditional skip instructions
  output [1:0] PC_Sel,
  output Push, Pop;
  // implementation details are left to the student
  …
endmodule
```

Additionally, you need to build simple combinational circuits to take care of the following:

1) The write enable of the Working register in the datapath should be a function of the “d” bit (IR_Data[7]), the W_write control signal, and the Write_en control signal.
2) The IR_Res signal in the program memory should be a function of the processor Reset signal, the IR_clear control signal, and the IR_clear_cond control signal.
3) The DataWrite signal in the data memory should be a function of the “d” bit (IR_Data[7]), the F_write control signal, and the Write_en control signal.

Report

Your report should include detailed design and Verilog code for all modules. Additionally, you need to determine the contents of the Control Memory. For this purpose, you need to complete the following table:

Location	Instruction	W_write	Write_en	M[3:0]	L_or_F	F_write	C_en	DC_en	Z_en	IR_clear	IR_clear_cond	PC_Sel[1:0]	Push	Pop
00 0000	movwf, nop	0	1	1101	x	0	0	0	0	0	0	00	0	0
00 0001	clrf, clrw	0	1	1100	x	0	0	0	1	0	0	00	0	0
00 0010	subwf													
00 0011														
00 0100														
00 0101														
00 0110														
00 0111														
00 1000														
00 1001														
00 1010														
00 1011														
00 1100														
00 1101	rlf	0	1	1001	1	0	1	0	0	0	0	00	0	0
00 1110														
00 1111														
01 0000														
01 0001														
01 0010														
01 0011														
01 0100														
01 0101														
01 0110														
01 0111														
01 1000														
01 1001														
01 1010														
01 1011														
01 1100														
01 1101														
01 1110														
01 1111														
10 0000	call	0	0	xxxx	x	0	0	0	0	1	0	01	1	0
10 0001	call	0	0	xxxx	x	0	0	0	0	1	0	01	1	0
10 0010	call	0	0	xxxx	x	0	0	0	0	1	0	01	1	0
10 0011	call	0	0	xxxx	x	0	0	0	0	1	0	01	1	0
10 0100	call	0	0	xxxx	x	0	0	0	0	1	0	01	1	0
10 0101	call	0	0	xxxx	x	0	0	0	0	1	0	01	1	0
10 0110	call	0	0	xxxx	x	0	0	0	0	1	0	01	1	0
10 0111	call	0	0	xxxx	x	0	0	0	0	1	0	01	1	0
10 1000														
10 1001														
10 1010														
10 1011														
10 1100														
10 1101														
10 1110														
10 1111														
11 0000														
11 0001														
11 0010														
11 0011														
11 0100														
11 0101														
11 0110														
11 0111														
11 1000														
11 1001														
11 1010														
11 1011														
11 1100														
11 1101														
11 1110														
11 1111														