University of Jordan
Computer Engineering Department
CPE439: Computer Design Lab

Experiment 8: The Processor Module

It is required to construct a Verilog module for the entire PIC16F84A processor. This module should include the three modules that you have constructed in the previous experiments, namely: datapath module, program memory module, and data memory modules. Additionally, the processor module should include a fourth module for the control unit.

This module should have Verilog code similar to the following code:

```
module Processor(PortA, PortB, Clock, Reset);
  inout [4:0] PortA;
  inout [7:0] PortB;
  input Clock, Reset;
  // implementation details are left to the student
  …
endmodule
```

Report

Your report should include detailed design and Verilog code for all modules.