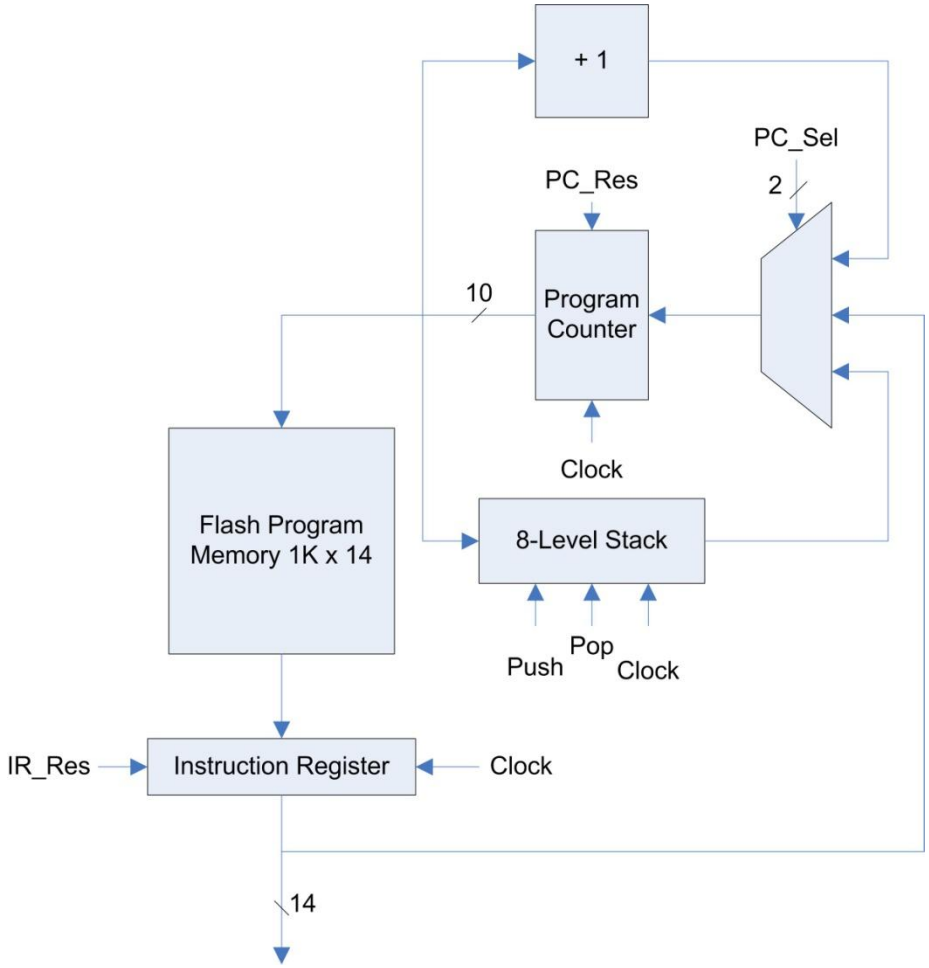
University of Jordan
Computer Engineering Department
CPE439: Computer Design Lab

Experiment 5: Program Memory Module

It is required to construct and test a Verilog module for a program memory suitable for incorporation in your PIC16F84A design. You should use modular design where you start by building and testing low-level modules using the library modules defined in **Lib439.v**, then use the low-level modules in larger modules. You can also reuse some of the modules that you have designed in previous experiments. The following figure shows the design of this program memory module.



This module should have Verilog code similar to the following code:

```
module ProgramMemory(IR_Data, Clock, IR_Res, PC_Res, PC_Sel, Push, Pop);
  output [13:0] IR_Data;
  input Clock;
  input IR_Res, PC_Res;
  input PC_Sel;        //0: PC+1, 1: IR_Data[9:0], 2: Stack
  input Push, Pop;
  // implementation details are left to the student
  …
endmodule
```

Flash Program Memory

The flash program memory should be implemented using behavioral modeling as follows:

```
//
// Flash Program Memory, 1K x 14 bits
//
module FlashProgramMemory(Dout, addr);
   output [13:0] Dout;
   reg [13:0] Dout;
   input [9:0] addr;

   reg [13:0] MA [1023:0];   //Storage array

   initial begin: InitContents
     // initialize the machine code of your instructions here
     MA[0] = 14'b00000000000000;
   end

   always @(addr) #8 Dout = MA[addr];

endmodule
```

8-Level Stack

The 8-level stack module should include stack pointer, incrementer, decrementer, and memory array. The memory array should be implemented using behavioral modeling as follows:

```
//
// Stack memory array, 8 x 10 bits
//
module StackMemoryArray(Dout, clock, wt, addr, Din);
   output [9:0] Dout;
   reg [9:0] Dout;
   input clock, wt;
   input [2:0] addr;
   input [9:0] Din;

   reg [9:0] MA [7:0];    //storage array

   always @(addr) #4 Dout = MA[addr];

   always @(posedge clock)
     if (wt == 1)
       #1 MA[addr] = Din;

endmodule
```

Report

Your report should include detailed design, Verilog code for all modules including your test modules, and timing diagram that demonstrates the correct operation of your design.