

University of Jordan
Computer Engineering Department
CPE439: Computer Design Lab

Experiment 10: Full Processor Simulation

It is required to test your design for the entire processor using the instruction sequence shown in the following table. This instruction sequence reads a number from Port A, outputs it to Port B, and keeps decrementing this number until it reaches zero. Finally, it outputs 8 ones to Port B.

Location	Instruction	Instruction Code
00	<code>call 05</code>	10 0000 0000 0101
01	<code>compf portb,1 ;set Port B</code>	
02	<code>nop</code>	
03	<code>nop</code>	
04	<code>nop</code>	
05	<code>bsf status,5</code>	
06	<code>movlw B'00011111'</code>	
07	<code>movwf trisa ;all input</code>	
08	<code>clrf trisb ;all output</code>	
09	<code>bcf status,5</code>	
0a	<code>clrf portb ;clear Port B</code>	
0b	<code>movf porta,0 ;get number</code>	
0c	<code>movwf portb ;output number to Port B</code>	
0d	<code>decfsz portb</code>	
0e	<code>goto 0d</code>	
0f	<code>return</code>	
10	<code>nop</code>	

To carry out this test you need to perform the following steps:

- 1) Instantiate your processor module in a test module.
- 2) The test module should provide to the processor initial reset signal and square wave clock of period suitable for your design.
- 3) The control memory must be initialized with all the needed control signals as specified in Experiment 9.
- 4) Complete the instruction codes in the table above and use these codes to initialize the program memory.
- 5) Port A should be processor input port and Port B should be processor output port. Your test module should set Port A to value B'00011' and monitor Port B.
- 6) You need to calculate the number of cycles needed to execute the above code sequence and stop your simulation as soon as the processor finishes executing the complement instruction.

Report

Your report should include detailed design and Verilog code for all modules, critical path analysis, and timing diagrams that demonstrate the correct operation of your design.