0907432 Computer Design (Spring 2010)

Quiz 2B

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Instructions: Time **15** minutes. Closed books and notes. No calculators. Please answer all problems in the space provided. **No questions are allowed**.

<Good Luck>

Q1. Calculate the average time to read a 4-KB sector for the disk with the following characteristics:

Average seek time	RPM	Disk Transfer Rate	Controller Transfer Rate
9 ms	7200	30 Mbytes/s	500 MBits/s

Average read time = seek time + rotational delay + transfer time
= 9 ms + 0.5 * (60/7200) + 4KB/30MB/s
= 9 ms + 0.5 * (1/120) * 1000 ms + 4/30 ms
= 9 ms + 500/120 ms + 4/30 ms
= 9 ms + 12.5/3 ms + 2/15 ms
= 9 ms + 4.17 ms + 0.13 ms
= 13.2 ms

Q2. Chip multiprocessor on-chip L2 cache design has interesting tradeoffs. The following tables show the miss rates and hit latencies for two benchmarks with private versus shared L2 cache designs. Assume L1 cache misses once every 32 instructions.

	Private	**Shared**
Benchmark A misses-per-instruction	0.30%	0.12%
Benchmark B misses-per-instruction	0.06%	0.03%

Hit Latencies:

Private Cache	**Shared Cache**	**Memory**
8 cycles	20 cycles	120 cycles

What cache design is better for each of these benchmarks? Use data to support your conclusions.

For private cache, use:
private miss rate × memory hit latency + (1 – private miss rate) × private cache hit latency

For shared cache, use:
shared miss rate × memory hit latency + (1 – shared miss rate) × shared cache hit latency

Benchmark A private: 0.003 × 120 + 0.997 × 8 = 0.36 + 7.976 = 8.336
Benchmark B private: 0.0006 × 120 + 0.9994 × 8 = 0.072 + 7.9952 = 8.0672
Benchmark A shared: 0.0012 × 120 + 0.9988 × 20 = 0.144 + 19.976 = 20.12
Benchmark B shared: 0.0003 × 120 + 0.9997 × 20 = 0.036 + 19.994 = 20.03

For both benchmarks, private cache design is better.