0907432 Computer Design (Spring 2010)

Quiz 1B

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Instructions: Time **20** minutes. Closed books and notes. No calculators. Please answer all problems in the space provided. **No questions are allowed**.

<Good Luck>

Q1. The following table shows results for SPEC2006 benchmark programs running on an AMD processor.

Name	Instr. Count x 10^9	Execution Time	Reference Time
perl	2118	500 s	9770 s
mcf	336	1200 s	9120 s

For these two benchmarks, find the geometric mean.

SPECratio = ref. time/execution time.

SPECratio(pearl) = 9770/500 = 19.54

SPECratio(mcf) = 9120/1200 = 7.6

Geometric Mean = $(19.54 \times 7.6)^{1/2} = 12.19$

Q2. The branch outcome of one branch instruction was (T, T, T, NT, NT). What are the accuracies of the following branch predictors on this branch instruction?

A) Always-taken predictor

B) Always-not-taken predictor

C) Two-bit predictor assuming that the predictor starts in the deep state of predict not taken

D) Two-bit predictor when the predictor executes this pattern repeatedly forever

A) Always-taken
3/5 = 60%

B) Always not-taken
2/5 = 40%

C) Outcomes	Predictor value at prediction	Correct or Incorrect	Accuracy
T, T, T, NT, NT	0, 1, 2, 3, 2	I, I, C, I, I	20%

D) The first few recurrences of this pattern do not have the same accuracy as the later ones because the predictor is still warming up. To determine the accuracy in the "steady state", we must work through the branch predictions until the predictor values start repeating (i.e. until the predictor has the same value at the start of the current and the next recurrence of the pattern).

Outcomes	Predictor value at prediction	Correct or Incorrect	Accuracy
T, T, T, NT, NT	1st occurrence: 0, 1, 2, 3, 2 2nd occurrence: 1, 2, 3, 3, 2 3rd occurrence: 1, 2, 3, 3, 2	I, C, C, I, I	40%

Q3. Consider the following loop

```
Loop:   lw    r1, 0(r2)
        lw    r3, 1000(r2)
        add   r1, r1, r3
        sw    r1, 2000(r2)
        addi  r2, r2, -4
        bne   Loop
```

A) Unroll this loop two times. You must remove unnecessary loop-control overhead and do needed instruction modifications to ensure correctness.

```
Loop:   lw    r1, 0(r2)
        lw    r3, 1000(r2)
        add   r1, r1, r3
        sw    r1, 2000(r2)
        lw    r1, -4(r2)
        lw    r3, 996(r2)
        add   r1, r1, r3
        sw    r1, 1996(r2)
        addi  r2, r2, -8
        bne   r2, zero, Loop
```

B) Perform any needed register renaming and schedule the unrolled loop to minimize stalls on a typical five-stage MIPS pipeline that resolves branches in the Execute stage and has full forwarding paths.

```
Loop:   lw    r1, 0(r2)
        lw    r3, 1000(r2)
        lw    r4, -4(r2)
        add   r1, r1, r3
        lw    r5, 996(r2)
        sw    r1, 2000(r2)
        addi  r2, r2, -8
        add   r4, r4, r5
        sw    r4, 2004(r2)
        bne   r2, zero, Loop
```