0917432 Computer Architecture and Organization 2 (Spring 2024)

Quiz 2

الشعبة: رقم التسجيل: الاسم:

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Instructions: Time **15** minutes. Open book and notes exam. No electronics. Please answer all problems in the space provided and limit your answer to the space provided. There are three problems. No questions are allowed.

P1. Assume that you have a modern processor that features powerful SIMD instructions and has register and cache data bus widths of 512 bits. What is the minimum number of SIMD load instructions needed to load a 128-element vector containing single-precision floating-point numbers (4 bytes each)?

<1.5 marks>

Solution:

Register/bus width in bytes = 512 bits / 8 bits/byte = 64 bytes

Elements per SIMD load = 64 bytes / 4 bytes/element = 16 elements

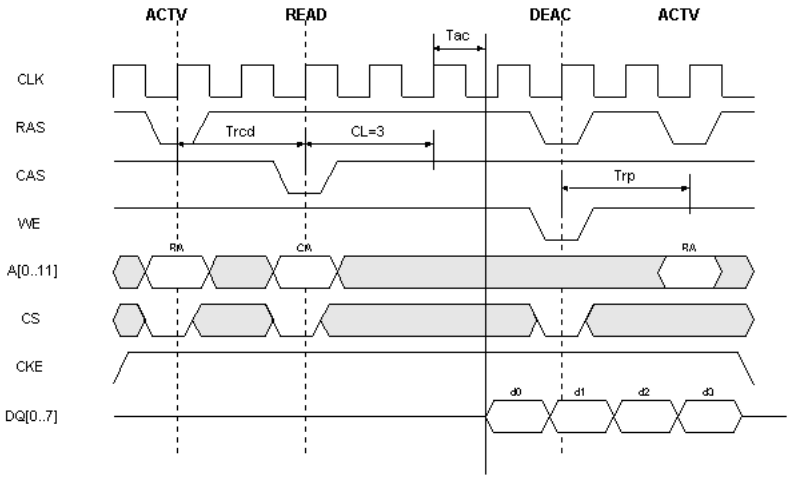
No. of SIMD loads = 128 elements / 16 elements/instruction = 8 load instructions

P2. Consider the following timing diagram of a memory chip and answer the following two questions.

<2 marks>

1) What is the type of this memory chip? _____**SDRAM**_____

2) How many data bits are accessed in this diagram? _____ **4 accesses * 8 bits = 32 bits** _____



P3. The size (data capacity) of a four-way associative cache is 32 KB. Assuming that the block size is 64 bytes, what is the width in bits of the address index field?

<1.5 marks>

Solution:

Number of blocks = 32 KB / 64 bytes/block = 512 blocks

Number of sets = 512 blocks / 4 blocks/set = 128 sets

Index field width = $\lg_2 128$ = 7 bits

<Good Luck>