0907432 Computer Design (Fall 2014) <u>Quiz 2</u>	
الاسم: رقم التسجيل: الرقم التسلسلي:	
<u>Instructions</u> : Time 20 minutes. Open book and notes exam. No electronics. Please answer all problems the space provided and limit your answer to the space provided. No questions are allowed. <i>Good Luck</i>	in
Q1. Assume that you want to design a 4-way associative cache and the size of this cache is 32 KB. [5 mark	ks]
A) How many blocks does this cache have if the block size is 64 bytes?	
Number of blocks = Cache size / block size	
= 32 KB / 64 B = 512 blocks	
B) How many bits are needed to index this cache? <index> = lg₂ (Number of blocks / Associativity)</index>	
$= lg_2 (512 / 4)$	
$= lg_2 (128) = 7 bits$	
C) What is the tag width if the address width is 32 bits?	
<tag> = 32 - <index> - <block offset=""></block></index></tag>	
$= 32 - 7 - \lg_2(64)$	
= 32 - 7 - 6 = 19 bits	
D) Assuming that this cache is a write-back cache and uses random replacement, how many memory bits are needed to construct this cache?	
Cache memory size = Number of blocks × Number of block bits	
= 512 × (<valid> + <dirty> + <tag> + <data>)</data></tag></dirty></valid>	
$= 512 \times (1 + 1 + 19 + 64 \times 8)$	

 $= 512 \times (21 + 512) = 512 \times 533$ bits

